AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows, without prejudice or disclaimer to continued examination on the merits:

Please make the following correction to paragraph [0003]:

[0003] Generally, in amorphous silicon flat panel x-ray detectors, an amorphous silicon array is disposed on a glass substrate, and a scintillator is ~~diposed~~ disposed over the amorphous silicon array. The scintillator converts x-ray photons to visible light, and then the amorphous silicon array converts the light into electrical charge. The charge at each pixel on the amorphous silicon array is then read out digitally by low-noise electronics, and is sent to an image processor. Thereafter, the image is displayed on a display, and may also be stored in memory for later retrieval.

Please make the following correction to paragraph [0004]:

[0004] The amorphous silicon array comprises field effect transistors (FETs) and photodiodes, typically arranged in rows and columns, wherein the FETs act as switches to control the charging of the photodiodes. The source of each FET is connected to a photodiode, and the drain of each FET is connected to readout electronics via ~~datalines~~ data lines or contact leads.

Please make the following correction to paragraph [0025]:

[0025] Referring now to Figure 3, there is shown a simplified equivalent circuit diagram 40 showing the pixel and readout electronics utilized in embodiments of this invention. As shown herein, a pixel is represented by a photodiode 41 and a scan switch 42 (which is actually a FET), where 50 represents the boundary between the panel and the electronics behind the panel. A ~~dataline~~ data line 43 connects each pixel to the circuitry

in the readout circuit. The readout circuit comprises an operational amplifier charge integrator 49, followed by a sample and hold circuit 46. Generally, a readout cycle starts with a reset pulse generated by briefly closing reset switch 44, which discharges the signal in the feedback capacitor 45 that is left from the previous readout cycle. Then, the pixel signal is integrated to the feedback capacitor 45 during the FET-on period (i.e., when scan switch 42 is closed). After the FET is switched off (i.e., after the scan switch 42 is open), the integrator output is sampled to the sample capacitor 47. This is essentially a full cycle sampling method, since the sample is taken after a full FET on/off cycle. The final signal that is stored in the feedback capacitor 45 includes the pixel charge, as well as the FET-on and FET-off transient charges, which capacitively couple to the data from the gate electrode of the FET. Because the FET-on and FET-off transient charges are equal in magnitude, but opposite in polarity, they cancel each other out in the final signal, which results in a very narrow offset dispersion. This circuit also comprises two grounds 48.

Please make the following correction to paragraph [0026]:

[0026] In this full cycle sampling method, once the FET is turned off (~~i.e~~ i.e., when scan switch 42 is opened), a charge is temporarily retained in the FET. This transient retained charge bleeds out, or decays, over time, which corrupts the signal being sent to the image processor. Therefore, a certain amount of settling time is necessary before signal sampling can occur. As this settling time can take up a significant portion of the total available readout time (i.e., in some cases, it can take up to 1/3 of the total available readout time), reducing or eliminating this settling time will free up more time for signal sampling and/or shorten the line time. Reducing the line time is key to achieving desirable high frame rate imaging (i.e., more than 30 frames/second).

Please make the following correction to paragraph [0027]:

[0027] Referring now to Figure 4, there is shown a timing diagram showing the timing of a conventional sampling scheme 60. Generally, in existing amorphous silicon flat panel x-ray detectors, a readout cycle is begun by closing the reset switch 61 to discharge any signal that may be left in the feedback capacitor 45 from the previous readout cycle. Thereafter, sampling/scanning is generally done for about 20μsec (i.e., by closing the scan switch 62 so that the FET is on for about 20μsec). Thereafter, about 10-20μsec of settling time is required (~~i.e~~ i.e., the scan switch is opened 63 so that the FET is off for about 10-20μsec). Then, just before a signal is sampled, the sample and hold switch is closed 64 to allow current to flow to the sample capacitor 47. Once a signal sample is obtained 65 at time=t+1, then the reset switch may be closed again 61 to discharge the signal in the feedback capacitor 45 before beginning another readout cycle. Then, the same cycle just described would be repeated.

Please make the following correction to paragraph [0028]:

[0028] Referring now to Figure 5, there is shown a timing drawing showing the timing of the novel sampling scheme utilized in embodiments of this invention. In this invention, a readout cycle is begun by closing the reset switch 91 to discharge any signal that may be left in the feedback capacitor 45 from the previous readout cycle. Thereafter, sampling/scanning is generally done for about 20μsec (i.e., by closing the scan switch 92 so that the FET is on for ~~about20μsec~~ about 20μsec). In this invention, there is no settling time required, and the FET-on transient charge is not cancelled before sampling. Just before a signal is sampled, and while the FET is still on 92, the sample and hold switch is closed 94 to allow current to flow to the sample capacitor 47. As soon as the sample and hold switch is opened again 96, the signal is sampled 95 while the FET is still on at time=t+1. Just after a signal sample is obtained 95, then the reset switch may be closed again 91 to discharge the signal in the feedback capacitor 45 before beginning another readout cycle. Shortly thereafter, and while the reset switch is still closed, the scan switch can be opened again 93 so that the FET is off. Then, the same cycle as just described would be repeated.